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Insightful Analysis of Processor Technology

FD-SOI OFFERS ALTERNATIVE TO FINFET

GlobalFoundries Leads With Cost-Sensitive Manufacturing Option

By Linley Gwennap (August 15, 2016)

Although many high-performance chips have forged ahead to expensive FinFET manufacturing nodes, others continue to use 28nm planar technology because of its low cost per transistor. But these latter products have been stuck at 28nm, in some cases for years, without any manufacturing options for improving their cost or power. With Moore's Law breached, GlobalFoundries is offering a new technology that could fill this gap.

FD-SOI is a variant of silicon-on-insulator (SOI) technology that adds a very thin oxide layer beneath the silicon transistor, as Figure 1 shows, greatly reducing leakage current versus traditional bulk CMOS. The new SOI version requires no doping in the channel, making it fully depleted (FD). It also enables operation at lower voltages than planar CMOS transistors can achieve, reducing active power.

As a planar (flat) technology, FD-SOI requires fewer processing steps than FinFET nodes to form the transistor; it also requires less double patterning. As a result, the processing cost for FD-SOI is lower. Although the SOI wafers are much more expensive than plain CMOS wafers, GlobalFoundries says its 22nm FD-SOI process, called 22FDX, can deliver lower die cost than 16nm FinFET. The new process is similar in die cost to 28nm HKMG while greatly reducing power.

These advantages make 22FDX particularly appealing for many IoT products that require the lowest possible cost but must also minimize power. In addition, the technology has some interesting analog characteristics. Samsung and STMicroelectronics also offer FD-SOI, but neither TSMC nor Intel favors this approach.

The Second Coming of SOI

SOI has been in production since the 1990s (see [MPR 8/24/98](#), "SOI to Rescue Moore's Law"). IBM brought the industry's first SOI-based processors to production in 2000, and AMD adopted the technology for all of its x86 microprocessors starting in 2001. Since then, IBM has continued to use SOI for many of its internal processors and also in its ASIC offerings, including processors for the PlayStation 3, Xbox 360, and Wii game consoles. AMD steadfastly rode the technology from 130nm all the way down to 32nm. After spinning off from AMD (see [MPR 9/27/10](#), "GlobalFoundries Pushes Boundaries"), GlobalFoundries continued to manufacture AMD's SOI designs. It recently acquired IBM's fabs, giving it additional SOI resources.

Instead of building directly on a bulk silicon wafer, SOI starts with a wafer that is topped with a layer of silicon oxide (an insulator). Another silicon layer (typically 150nm thick) is placed on the insulator before the wafer ships to the foundry, which constructs the transistors and other circuits in the usual fashion. Owing to the process of

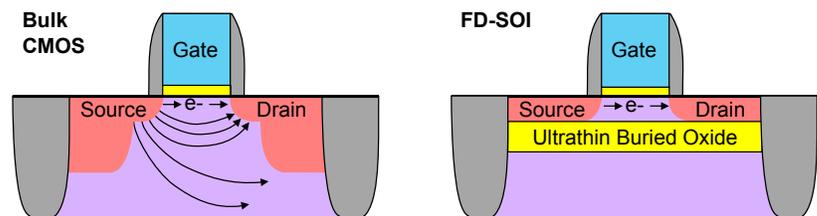


Figure 1. Traditional CMOS versus FD-SOI. As a bulk-CMOS transistor gets smaller, electrons can jump from the source to the drain even when the gate is off, creating leakage current. In the FD-SOI transistor, the buried oxide layer blocks most of the leakage.

adding the extra layers, SOI wafers cost considerably more. Soitec (pronounced “soy-tek”), the leading manufacturer of SOI wafers, declines to publish its prices, but we estimate them at \$400–\$500, as opposed to about \$130 for a bulk wafer.

From an electrical standpoint, the oxide barrier completely isolates the transistor body from the base substrate (ground). The floating body can thus accumulate charge over time, changing its threshold voltage. Removing the dopant from the channel (thereby fully depleting it) eliminates its ability to hold charge, solving the floating-body problem. But undoped transistors are highly sensitive to variations in the silicon-layer thickness. To simplify manufacturing, IBM and AMD originally implemented a partially depleted (PD) channel, but the floating-body effect complicated the circuit design of their PD-SOI processors.

On the plus side, the insulating layer greatly reduces source and drain capacitance, minimizing the power spent charging these capacitors. As a result, in early PD-SOI nodes such as 180nm, dynamic (switching) power dropped by about 50% at the same speed, or the speed increased by 25%. As transistors shrank over time, however, so did PD-SOI’s benefits; the speed gain is negligible at 28nm.

More recently, Soitec developed a technique to deposit a much thinner (e.g., 15nm) silicon layer with just 3% variance (5 angstroms). To take advantage of this work, the French company began working with a local partner, STMicroelectronics, to develop a complete manufacturing process. The highly consistent silicon thickness enabled ST to fully deplete the channel. In 2014, the company deployed the new 28nm FD-SOI process in its Crolles (France) fab, licensing the technology to Samsung as a second source.

GlobalFoundries (GF) also licensed ST’s FD-SOI technology. But instead of bringing it directly to production, GF melded the technology with its own SOI developments and advanced fabrication techniques to create a 22nm FD-SOI process. It expects to achieve low-volume production in 1Q17, with initial customer products entering full production around 2H17.

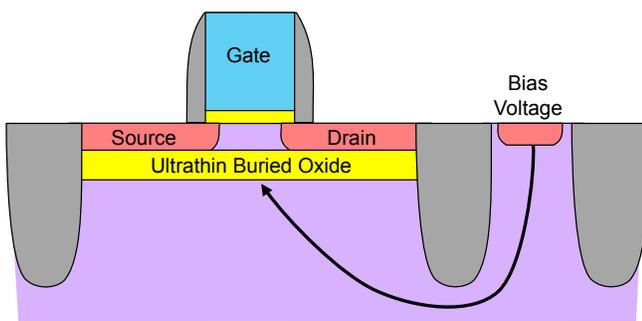


Figure 2. Body bias in FD-SOI. Applying a bias voltage can reduce the threshold voltage of the transistor, causing it to switch faster.

Lower Power Than Planar CMOS

A major benefit of FD-SOI is its low power. Because the circuit need not charge the source/drain capacitance, the total dynamic power falls. Furthermore, unlike ST’s original FD-SOI design, 22FDX uses a compressively strained channel in the PFETs as well as raised source drains in both the NFETs and PFETs. These optimizations reduce power by up to 55% compared with 28nm FD-SOI at the same frequency. GF has tested 22FDX designs down to 0.3V operation, although it has determined the minimum power occurs at 0.4V because leakage current begins to dominate below that point. Even so, 0.4V compares favorably with 28nm LP transistors, which typically reach minimum power at 0.65V.

Operating the transistors at this low voltage requires body biasing. As Figure 2 shows, applying a bias voltage to the substrate below the transistor affects the voltage of the body, causing the transistor to switch at a lower effective voltage. (Bulk-CMOS processes also employ body bias, but the effect is smaller.) The use of body biasing is optional in 22FDX, as the bias generators and extra routing add 2–3% to the die area. A forward bias (positive voltage) reduces the threshold voltage (thereby raising the switching speed) but increases leakage current, whereas a reverse bias reduces static leakage when high performance is unnecessary. A chip can dynamically adjust the bias voltage—for example, when it enters a low-power sleep mode—to optimize power consumption.

Like some other GF processes, 22FDX is constructed gate first. This approach simplifies analog integration, making the technology well suited to mixed-signal SoCs. Although some gate-first processes have suffered yield problems, GF expects the defect rate (per mm²) will be similar for 22FDX and its previous 28nm HKMG node.

The combination of gate-first design and SOI also improves certain analog characteristics. For example, the process has a high ratio of transconductance to drive current (Gm/I), reducing power in circuits such as power amplifiers and RF dividers. Furthermore, the faster transistors are well suited to high-frequency RF signals. GF has measured a maximum oscillation frequency (Fmax) in excess of 310GHz, and it expects further improvement. RF transistors must operate at 3x to 5x the base frequency, so 22FDX can easily handle millimeter-wave applications such as the new 5G radio (see [MCR 8/8/16](#), “U.S. Government Acts on 5G”), satellite communications, microwave backhaul, and radar.

Less Expensive Than FinFETs

Despite its prior focus on PD-SOI, GlobalFoundries has developed bulk-CMOS processes at the 28nm node and beyond. Its first FinFET offering, a 14nm technology that it licensed from Samsung, is now in production, with customer products ramping later this year. The company plans to skip 10nm and deploy a 7nm FinFET process that

is scheduled for production by the end of 2018, with customer products ramping in 2019. These advanced nodes target high-performance devices such as AMD's PC processors, but the cost of achieving this performance level continues to rise.

The 22nm FD-SOI process logically fits between GF's 28nm and 20nm technologies. Compared with 28SLP (a 28nm HKMG process), 22FDX reduces the gate pitch by 9% to 104nm, a size that a single patterning cycle (litho-etch) can still manage. The new technology offers a total of eight metal layers. The only two layers in the entire process that require double patterning are the first two metal layers, which have an 80nm pitch, as Table 1 shows. The 11% metal shrink and 9% gate shrink don't add up to a full node; the company estimates die area will fall by 20% on average rather than the 40–50% of a traditional node shrink.

The effect on die cost is more complex. The double-patterning restriction helps limit the processing-cost increase, but that cost is still greater than for 28HPP. The SOI wafer cost is also greater, but the smaller area improves both die per wafer and yield for a straight product shrink. According to GF's calculations, 28HPP and 22FDX will have similar cost per die for most designs. Yet FD-SOI offers a sizable power reduction owing to the lower operating voltage and decreased leakage current. In fact, the company believes 22FDX, using a special transistor layout, can achieve leakage similar to that of TSMC's 40nm ULL (ultra-low-leakage) CMOS technology—a popular choice for battery-powered products.

GF has also benchmarked 22FDX against its own 14nm FinFET technology (see [MPR 2/2/15](#), "Foundries Find FinFETs at 14nm"). The three-dimensional FinFETs produce more drive current for a given footprint than the planar 22FDX transistors, making them better for high-frequency designs and for large chips than must drive signals across long wires. At the same operating frequency, the 14nm FinFETs also leak less than 22FDX transistors. But the lower source/drain capacitance for 22FDX reduces the active power below that of 14LPP, making the total power similar in some lower-frequency designs. In addition, the planar 22nm technology has far fewer design rules than FinFET processes, easing the design task. This simplification is particularly attractive for lower-volume designs.

Although FinFET nodes are generally considered to have a higher per-transistor cost than 28nm, die cost varies as a function of area. For large die, the area shrink from the smaller 14nm transistors and tighter metal pitches generally results in a lower die cost when using 14LPP. For die smaller than 120mm² (in 22nm), particularly those with significant analog or RF content, 22FDX's lower per-wafer cost makes it more economical. In these cases, the FD-SOI process offers a cheaper alternative to FinFET technology while providing similar power benefits.

Price and Availability

GlobalFoundries' 22FDX process is expected to begin risk production 4Q16; full production is expected in 1Q17, leading to customer volume production in 2H17. The company withheld wafer pricing. For more information, access www.globalfoundries.com/22fdx.

FD-SOI Gains Design Wins

Over the past two decades, PD-SOI technology made some progress but never achieved widespread adoption. Back when a fully processed wafer sold for \$1,500 or \$2,000, few chip makers were willing to pay a few hundred dollars extra for an SOI wafer. Today, a fully processed FinFET wafer costs around \$7,000, so the FinFET cost premium is considerably larger than the SOI premium. Furthermore, technology improvements allow Soitec to produce ultra-thin-layer wafers that enable fully depleted SOI processes, simplifying chip design compared with the older partially depleted processes.

FinFET has supplanted PD-SOI as the technology of choice for high-performance cost-insensitive products. But GlobalFoundries' new 22nm FD-SOI technology offers a lower-cost alternative, at least for smaller die that operate at moderate clock speeds. The 22FDX process is also superior to 28nm for analog-heavy designs and for high-frequency RF products. Chip vendors that want to upgrade their 28nm HKMG products can move to 22FDX at about the same cost per die while garnering significant power benefits.

STMicroelectronics has seen little uptake for its pioneering 28nm FD-SOI technology, which offers lower power than 28nm HKMG but costs more. In fact, it has chosen to forgo developing any IC processes below 28nm. As a more active foundry, Samsung is seeing greater interest in 28nm FD-SOI, reporting 12 tapeouts in 2015 and expecting a similar number this year. One notable design win is NXP's i.MX8 automotive-infotainment processor. Even so, Samsung has not announced a roadmap for FD-

Model	28SLP	22FDX	20HPP	14LPP
Transistor Node	28nm	22nm	20nm	14nm
Transistor Type	HKMG	FD-SOI	HKMG	FinFET
Nominal V _{dd}	1.0V	0.8V	0.9V	0.8V
Minimum L _{gate}	30nm	20nm	20nm	20nm
Contacted Gate Pitch	114nm	104nm	90nm	78nm
Min Metal Pitch	90nm	80nm	64nm	64nm
HD SRAM Cell	0.120μm ²	0.110μm ²	0.081μm ²	0.064μm ²
Relative Die Area	100%	80%	63%	59%
First Customer Prod	2Q13	2H17	N/A*	2H16

Table 1. GlobalFoundries process technologies. The company's 22FDX offers a 20% die shrink from its 28nm node, but it's bigger than the 20nm and 14nm nodes, particularly for the metal layers. *GF never brought 20HPP to production, instead focusing on 14LPP. (Source: TechInsights, GlobalFoundries)

SOI at 22nm or below, instead focusing on FinFET technology for those nodes.

By contrast, GlobalFoundries skipped 28nm FD-SOI to focus on its 22nm technology. This approach provides an upgrade path for 28nm LP and HKMG products, particularly those seeking to reduce power (both active and leakage) without increasing die cost. Today, GlobalFoundries is the only purveyor of FD-SOI at 22nm, giving it a differentiated process.

Now that the economic progress of Moore's Law has stopped, chipmakers must find new innovation vectors to continue to advance performance. FD-SOI is no panacea; it primarily addresses the needs of low-cost IoT and other power-sensitive devices. But these applications comprise a sizable market, and GlobalFoundries' unique offering makes it a strong choice for them. Chip manufacturing is no longer one-shrink-fits-all, and FD-SOI could prove valuable for many products. ♦

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